Third-Order Intermodulation Distortion and Gain Compression in GaAs FET's

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Abstract—**A simple unilateral nonlinear circuit model of a GaAs FET is used in the analysis of the third-order intermodulation distortion and gain compression characteristics of a single-stage amplifier. Expressions are obtained for these characteristics, relating them to the input power level and to the device load admittance. The expressions are illustrated with contours on the load admittance plane of constant intermodulation distortion ratio, intercept point, gain compression, AM-to-PM conversion, and output power, and as output power versus input power plots for fixed terminations. Agreement with experimentally measured distortion characteristics is good.**

I. Introduction

IN RECENT YEARS there has been a strong trend towards the replacement of conventional traveling-wave-tube power amplifiers with solid-state units based on GaAs FET's. The analysis and design of these solid-state amplifiers requires that the nonlinear properties of the active devices are well characterized. For the GaAs FET, properties such as third-order intermodulation distortion (IMD) and output power under compressed-gain conditions can be obtained experimentally [1]. These measurements are carried out as a function of easily defined parameters such as the terminating admittances presented to the device and the power level of the input signal. Graphical design procedures can be developed easily on the basis of these data [1].

An alternative to the purely experimental approach is to use an analytical procedure based on either a nonlinear circuit model or an analytical model of the GaAs FET. This method gives a greater understanding of the mechanism of distortion. A number of authors [2]–[4] have undertaken analysis of this type, but their results are of limited application in the design of high-efficiency amplifiers. Khadr and Johnston [2], for example, carried out a third-order distortion analysis of a JFET using the Volterra series approach. Since their method assumes low distortion levels, gain compression is not taken into account. Perlow's analysis of third-order distortion [3] allows for gain compression. However, it does not incorporate a device circuit model, and thus it can not quantify the distortion characteristics in terms of the terminating impedances presented to the device. Tucker and Rauscher [4] found an analytical expression for the third-order IMD properties of a GaAs FET in terms of the load termination but ignored the effects of gain compression. The analysis of Willing *et al.* [7] is numerical and thus requires considerable computation time.

This paper investigates the third-order distortion properties of a single-stage GaAs FET amplifier based on a nonlinear unilateral circuit model. This circuit model incorporates nonlinearities in the gate, the transconductance, and at the output or drain of the device. Gain compression is accounted for, and the analysis thus applies for both small- and medium-signal input power levels.[1] Analytical expressions are obtained which relate the third-order IMD and gain compression to the load admittance and input power level. Normalized contours of constant gain compression and AM-to-PM conversion on the load admittance plane are given. Illustrative examples of contours of constant IMD, intercept point, gain compression, and output power are presented for a specific transistor.

The paper is organized as follows. The device circuit model is described, and its response to sinusoidal input signals is analyzed in Section II. This analysis is carried out in terms of power series expansions of device nonlinearities. Distortion characteristics such as third-order IMD and gain compression are defined in Section III, and the analytical expressions for these are obtained. Examples for a particular device are presented in Section IV.

II. Circuit Model

Fig. 1 shows the unilateral nonlinear device circuit model connected as an amplifier with an input (gate) termination admittance Y_s and a load admittance Y_L. Since a unilateral model for the FET is assumed, drain-to-gate feedback elements are neglected. This is a good approximation and enables one to consider first the input and output portions of the circuit separately and then to study their combined effect. It is assumed that there are four nonlinear circuit elements: the Schottky-barrier junc-

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[1]The term *small signal* is used here to refer to input power levels for which the device exhibits negligible gain compression. At input power levels where the output power is not proportional to the input power but where gain compression (or expansion) is less than about 2 dB, the device is said to be operating at *medium-signal* input levels. A further increase in input power level gives rise to *large-signal* operation.

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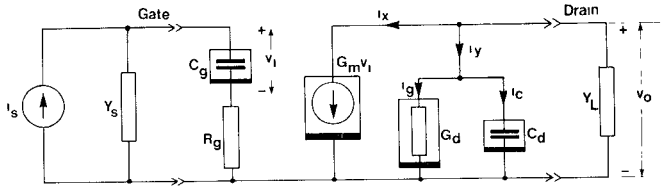

Fig. 1. Nonlinear circuit model of single-stage GaAs FET amplifier.

tion capacitance at the gate C_g, the gate-voltage-dependent transconductance G_m, the output-voltage-dependent drain conductance G_d, and the output-voltage-dependent drain capacitance C_d. The first two of these, C_g and G_m, are considered part of the *input circuit* since the current in both of these elements depends solely on the gate voltage v_i. The elements G_d and C_d are considered part of the *output circuit* since the currents i_g and i_c depend solely on the output voltage v_o.

Input Circuit

It has been shown [4] that the third-order IMD of a GaAs FET is virtually independent of the admittance Y_s at the input port. The transfer function of the input circuit can thus be written in a form which lumps together the nonlinear effects of C_g and G_m. It is expressed as a power series with order-dependent time delays [5]:

$$i_x(t)=\sum_{l=1}^{N} g_{ml} v_i^l(t-\tau_l) \tag{1}$$

where v_i and i_x are as shown in Fig. 1, g_{ml} are real expansion coefficients, and τ_l are time delays. The number of terms required in (1) depends upon the particular device under consideration. For some transistors it may be necessary to take terms in v_i up to the fifth order ($N=5$), but it has been found that for many devices $N=3$ gives an adequate approximation for small- and medium-signal operation. A value of 3 is used for N in the present analysis.

With the nonlinearity of the input circuit characterized, it is now necessary to determine the response of the circuit to an input signal. If the transistor is driven simultaneously by two closely spaced equal-amplitude unmodulated carriers (as in the so-called two-tone test), then the input voltage v_i can be written in the form

$$v_i(t)=A(\cos \omega_1 t+\cos \omega_2 t) \tag{2}$$

where A is a real constant, and ω_1 and ω_2 are the radian frequencies of the two carrier signals. This signal gives rise to components of the current i_x (Fig. 1) both at the two carrier frequencies ω_1 and ω_2 and at the two third-order IMD frequencies $(2\omega_1-\omega_2)$ and $(2\omega_2-\omega_1)$. It is shown in the Appendix that these currents are, in phasor notation,

$$I_{xc}=AH_1\left(1+\tfrac{9}{4}A^2H_3H_1^{-1}\right) \quad \text{(carrier)} \tag{3}$$

and

$$I_{xd}=\tfrac{3}{4}A^3H_3 \quad \text{(distortion)} \tag{4}$$

where

$$H_l=g_{ml}/\epsilon_l$$

and

$$\epsilon_l=-\omega_1\tau_l.$$

The first term in (3) represents linear device gain while the second term accounts for gain compression or expansion in the input circuit. For a single-carrier input of the form

$$v_i(t)=A\cos \omega_1 t \tag{5}$$

a similar procedure gives the carrier component of I_x at the frequency ω_1 as

$$I_{xc}=AH_1\left(1+\tfrac{3}{4}A^2H_3H_1^{-1}\right). \tag{6}$$

Output Circuit

The nonlinear drain conductance G_d and the nonlinear drain capacitance C_d are represented in power series form as follows:

$$i_g(t)=\sum_{l=1}^{N} g_l v_o^l(t) \tag{7}$$

and

$$i_c(t)=\sum_{l=1}^{N} c_l \frac{dv_o^l(t)}{dt} \tag{8}$$

where g_l and c_l are real expansion coefficients of the conductance and capacitance, respectively. As with the input circuit, distortion components of order higher than 3 are assumed to be negligible in the present analysis, and thus $N=3$. The signal distortion characteristics of the output circuit are obtained by substituting $v_o(t)$ as a sum of sinusoids into (7) and (8). However, before this is described, a further simplification of (7) and (8) is to be considered.

Components of third-order distortion due to G_d and C_d can be attributed to both the square-law and cubic terms in (7) and (8). Carrier-frequency components and third-order IMD components present in the output voltage v_o give rise to third-order distortion components in the currents i_g and i_c via the cubic terms. Similarly, second-harmonic distortion components of the carriers, at frequencies $2\omega_1$ and $2\omega_2$, in the output voltage v_o give rise to third-order distortion when combined with carrier-frequency signals and third-order IMD signals in the square-law terms. As explained previously [4], these interactions between second-harmonics and other spectral components of the output voltage have been experimentally investigated with a number of different GaAs FET's. It was found that second-harmonic distortion components have negligible effect on third-order distortion. Thus the second-order expansion coefficients g_2 and c_2, which give rise to second-harmonic distortion, can be assumed to be zero in the calculation of third-order distortion.

The experiments were carried out with the transistors operating in the class A mode and with a series of low-pass filters and adjustable-length coaxial lines connected at the output of the devices. It was thus possible to adjust

the carrier-frequency load admittance $Y_L(\omega_1)$ to a fixed value, and to simultaneously vary the second-harmonic load admittance $Y_L(2\omega_1)$ over a wide range of values. With variations in $Y_L(2\omega_1)$ and the consequent variations in second-harmonic output voltage, the third-order IMD remained almost constant.

In phasor notation, the carrier-frequency component and the third-order IMD component of the output voltage is V_{oc} and V_{od}, respectively. The corresponding components of the current I_y (Fig. 1) are shown in the Appendix to be

$$I_{yc} \simeq V_{oc} J_1 \left(1 + \tfrac{9}{4} J_3 J_1^{-1} |V_{oc}|^2\right) \quad \text{(carrier)} \tag{9}$$

and

$$I_{yd} \simeq V_{od} J_1 + \tfrac{3}{4} V_{oc} |V_{oc}|^2 J_3 \cdot \left(1 + 4 V_{od} |V_{oc}|^{-1}\right) \quad \text{(distortion)} \tag{10}$$

where

$$J_l = |J_l| \angle \sigma_l = g_l + j\omega_1 c_l.$$

For a single-tone input signal as given by (5), the carrier component of I_y is

$$I_{yc} = V_{oc} J_1 \left(1 + \tfrac{3}{4} J_3 J_1^{-1} |V_{oc}|^2\right). \tag{11}$$

III. Distortion Characteristics

In the previous section, nonlinearities in the GaAs FET circuit model were identified and the response of these nonlinearities to two-tone and single-tone input signals was described. It is the objective of this section to obtain analytical expressions for a number of distortion characteristics in terms of the input power level and the load admittance.

Gain Compression

The carrier-frequency component of output voltage V_{oc} can be expressed in terms of the input voltage by applying Kirchoff's current law at the device output. Using (3) and (9), and (6) and (11) for the two-tone and single-tone cases, respectively, the carrier-frequency output voltage is thus

$$V_{oc} = -\frac{AH_1 + \tfrac{3}{4} aA^3 H_3}{Y + \tfrac{3}{4} aJ_3 |V_{oc}|^2} \tag{12}$$

where $a = 1$ for single-tone input signals, and $a = 3$ for two-tone input signals. The admittance Y is given by

$$Y = Y_L + J_1$$

where J_1 is the small-signal output admittance of the device. The deviation of device gain from its small-signal value is characterized here by the parameter k, defined as the ratio of V_{oc} as given by (12) to V_{oc} under ideal linear conditions where $H_3 = J_3 = 0$:

$$k = \frac{-YV_{oc}}{AH_1}. \tag{13}$$

This parameter represents the ratio of the amplifier voltage gain at an arbitrary input signal level to the voltage gain at small-signal levels. In terms of power gain the corresponding parameter is $|k|^2$ which is referred to here as "gain compression." If $|k|^2 < 1$ the gain is reduced to a value below its small-signal value, while for $|k|^2 > 1$ the gain is increased or expanded.

The device carrier-frequency output power (per carrier for two-tone inputs) P_{out}, written in terms of the output voltage and load conductance, is

$$P_{\text{out}} = |V_{oc}|^2 G_L \tag{14}$$

where $Y_L = G_L + jB_L$. Combining (14) with (13), the output power can be written in the form

$$P_{\text{out}} = \frac{A^2 |H_1|^2 G_L}{|Y|^2} |k|^2 \tag{15}$$

or

$$P_{\text{out}} = P_{\text{in}} G_p |k|^2 \tag{16}$$

where P_{in}, which is proportional to A^2, is the input power per carrier and G_p is the small-signal (linear) power gain of the device. The small-signal power gain is a function of the load admittance and is given by

$$G_p = G_{pm} \frac{4 g_1 G_L}{|Y|^2} \tag{17}$$

where G_{pm} is the maximum small-signal power gain. The gain compression $|k|^2$ is a function of both the load admittance and the input power. From (15) to (17) the maximum small-signal power gain is

$$G_{pm} = \frac{A^2 |H_1|^2}{4 g_1 P_{\text{in}}}. \tag{18}$$

An expression for k can be obtained from (12), (13), and (18):

$$k = \frac{1 + aP_{\text{in}} B}{1 + aP_{\text{in}} D |k|^2 |Z|^2 Z} \tag{19}$$

where

$$B = 3 g_1 G_{pm} H_3 H_1^{-1} |H_1|^{-2} = |B| \angle (\epsilon_3 - \epsilon_1)$$

$$D = 3 g_1 G_{pm} J_3 = |D| \angle \sigma_3$$

and $Z = R + jX = Y^{-1}$. Note that, in (19), k is defined in terms of four independent device parameters, namely the magnitude and phase of B and D. The numerator of (19) represents the contribution of the input circuit to the value of k, and the denominator represents the corresponding contribution of the output circuit. It is thus convenient to write (19) in the form

$$k = k_i k_o \tag{20}$$

where

$$k_i = |k_i| \angle \phi_i = 1 + aP_{\text{in}} B \tag{21}$$

$$k_o = |k_o| \angle \phi_o = \left(1 + |k_o|^2 |z_n|^2 z_n\right)^{-1} \tag{22}$$

and z_n is a normalized impedance given by

$$z_n = r_n + jx_n = \left(aP_{\text{in}} |k_i|^2\right)^{1/3} |D|^{-2/3} DZ. \tag{23}$$

The gain compression due to the input circuit $|k_i|^2$ is given

by (21), a linear equation in P_{in}. Similarly, the gain compression due to the output circuit $|k_o|^2$ is obtained from the nonlinear (22). Since (22) is expressed in terms of the normalized impedance z_n, universal contours of constant $|k_o|^2$ can be obtained on the z_n plane and then applied to any transistor. Thus it is not necessary to solve (22) for each device.

Some contours of constant $|k_o|^2$ are shown on the normalized impedance plane z_n in Fig. 2. The curves were obtained by solving (22) numerically on a programmable pocket calculator using Newton's method and plotting the results point by point. Only the upper half of the z_n plane is shown since the contours are symmetrical about the r_n axis. Values of $|k_o|^2$ ranging from +3 dB (a gain increase or expansion) to −3 dB (a gain reduction) are given. As would be expected from (22), there is 0 dB of gain compression at the point $z_n=0$ which corresponds either to a short circuit at the drain terminals of the device or to zero P_{in}. Also shown in Fig. 2 is the direction of the R and X axes of the unnormalized impedance plane Z. This illustrates that there is an axis rotation associated with the magnitude normalization in (23).

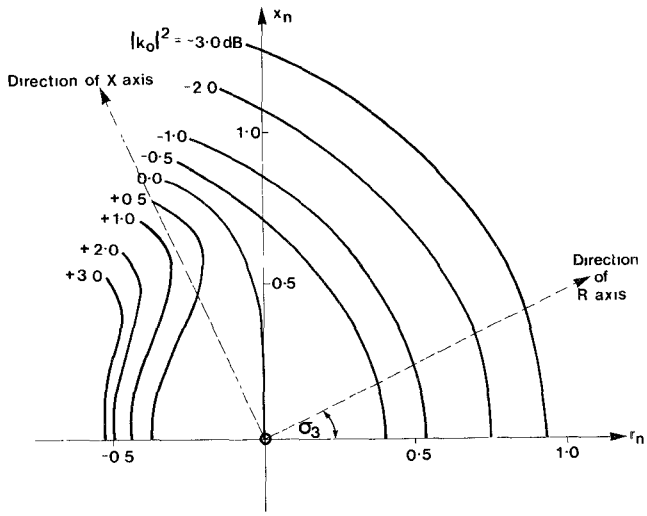

Fig. 2. Contours of constant output circuit gain compression $|k_o|^2$ on the normalized impedance plane z_n.

AM-to-PM Conversion

The instantaneous AM-to-PM conversion α of an amplifier is defined here as the rate of change of phase angle of the carrier-frequency output signal with changing input power level in decibels. For an FET with known terminations, the AM-to-PM conversion is found by differentiating the phase angle of k with respect to the logarithm of P_{in}:

$$\alpha=\frac{180}{\pi}\cdot\frac{d\phi}{d(10\log P_{in})} \quad \text{(degrees/dB)} \quad (24)$$

where

$$\phi=\phi_i+\phi_o$$

$$\phi_i=\tan^{-1}\left(\frac{awP_{in}}{1+avP_{in}}\right)$$

$$\phi_o=-\sin^{-1}\left(|k_o|^3|z_n|^2x_n\right)$$

and

$$B=v+jw.$$

From (20) to (24) it can be shown that

$$\alpha=|k_i|^{-2}\{13\cdot19awP_{in}+Q(|k_i|^2+2avP_{in})\} \quad \text{(degrees/dB)} \quad (25)$$

where

$$Q=\frac{13\cdot19|k_o|^2|z_n|^2x_n}{1+4r_n|k_o|^2|z_n|^2+3|k_o|^4|z_n|^4} \quad \text{(degrees/dB)}.$$

The first term in (25) represents the contribution of the input circuit to the overall AM-to-PM conversion while the second term represents the contribution of the output circuit. If the device parameter B is zero and thus there is no distortion in the input circuit, then the AM-to-PM conversion is equal to Q. Fig. 3 shows some contours of constant Q on the right-half normalized impedance plane z_n. As with the contours of Fig. 2, these curves can be applied to any transistor. It is interesting to note that the values of Q given in Fig. 3 are quite small, indicating that the output circuit has good AM-to-PM conversion characteristics. Comparing Fig. 3 with Fig. 2 in the right half z_n plane, it can be seen, for example, that for a gain compression of −1 dB, the value of Q is less than about ±3 degrees/dB.

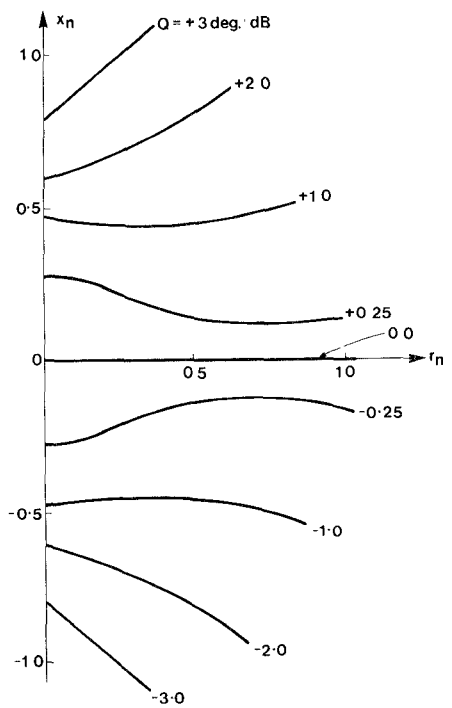

Fig. 3. Contours of constant Q on the normalized impedance plane z_n.

Intermodulation Distortion Ratio

The IMD voltage ratio R_{im} is defined as [3]

$$R_{im}=|V_{od}|/|V_{oc}|.$$

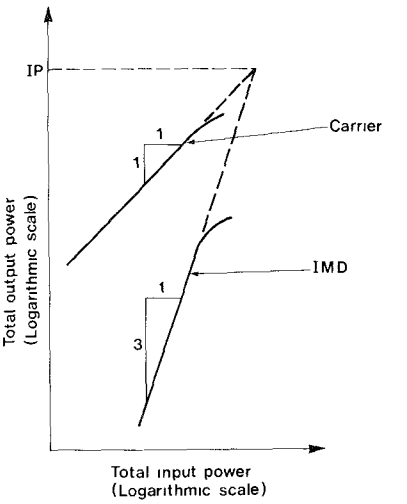

Fig. 4. Total output power versus total input power characteristic, showing intercept point.

It can be expressed in terms of P_{in} and the load by applying Kirchhoff's current law at the device output and from (4), (10), and (13):

$$R_{im}=\frac{P_{in}|B-\eta D|}{|k-4P_{in}H_1|H_1|^{-1}\eta D|}$$

where

$$\eta=|k|^2|Z|^2kZ.$$

This expression can be approximated by setting the denominator to unity and rearranging the numerator to give

$$R_{im}=P_{in}|E-\eta|D||| \tag{26}$$

where

$$E=B|D|D^{-1}=|B|\underline{/(\epsilon_3-\epsilon_1-\sigma_3)}\,. \tag{27}$$

For small signals, where k is close to unity, (26) can be further simplified to

$$R_{im}=P_{in}|E-|D||Z|^2Z|. \tag{28}$$

It is of interest to note that this expression describes identical small-signal third-order IMD characteristics to those given in [4] where the output capacitance was assumed to be linear.

The IMD characteristics described by the above expressions are directly related to the third-order coefficients in the power series (1), (7), and (8) by the parameters B and D. These parameters also affect the gain compression and AM-to-PM conversion characteristics. However, no simple relationship exists between IMD and either gain compression or AM-to-PM conversion.

Intercept Point

The third-order intercept point of an amplifier is a useful measure of its IMD performance in relation to the total output power. The definition of intercept point is illustrated in Fig. 4 which shows the total output power versus total input power characteristic of an amplifier driven by a two-tone signal. The intercept point is the point of intersection of straight-line extrapolations of the small-signal carrier output power and the small-signal IMD output power. As shown in Fig. 4, these lines have slopes of 1:1 and 3:1, respectively. It has been noted by Strid and Duder [8] that at large-signal levels, some GaAs power FET's exhibit deviations from the 3:1 slope. These deviations are partially due to coefficients of order greater than 3 in (1), (7), and (8). At small-signal levels, however, the higher order terms are negligible, and the slope of the IMD output power is always very close to the 3:1 value.

Since the total two-tone carrier output power is $2P_{out}$ and the total IMD output power is $2P_{out}R_{im}^2$, it follows directly from Fig. 4 that the output power at the intercept point IP is given by

$$IP=2P_{out}R_{im}^{-1}. \tag{29}$$

With (16), (17), (28), and $k=1$ since the intercept point is defined in terms of small-signal IMD, (29) becomes

$$IP=\frac{8g_1G_LG_{pm}}{|E|Y|^2-|D|Y^{-1}|}. \tag{30}$$

IV. Illustrative Examples

With the analytical expressions for gain compression and IMD derived, it is of interest to apply these expressions to a particular transistor. As shown earlier, the gain compression and AM-to-PM conversion due to the output circuit can be plotted in the form of normalized contours which can be applied to any transistor. However, IMD characteristics and output power contours do not lend themselves to normalization and are best illustrated with a specific example.

The first step in calculating the distortion characteristics of a given device is to obtain numerical values for the device parameters B, D, and E. This could be done on the basis of low-frequency measurements of each of the nonlinear elements in the device circuit model [2]. An alternative approach, which is better suited to the analysis presented here, is to obtain the parameters from measured distortion data at microwave frequencies. This straightforward method has some advantages over an analysis based on low-frequency measurements. In particular, it enables parameters to be determined as a function of frequency and thus allows for the effect of small parasitic elements in the device.

The transistor considered here has a gate width of 300 μm. This is a relatively low-power device, but demonstrates characteristics which have the same form as those of higher power devices. The major difference is simply a scaling of power and impedance level. All device parameters were obtained from measurements at microwave frequencies. The first of these measurements were of small-signal scattering parameters, giving $g_1=5.04$ μmho, $b_1=5.62$ μmho, and $G_{pm}=8.83$ dB at 10 GHz. Following this, E and $|D|$ were obtained from small-signal IMD measurements and B and $\underline{/D}$ were obtained from measured gain compression data. Details are given in the illustrative examples below.

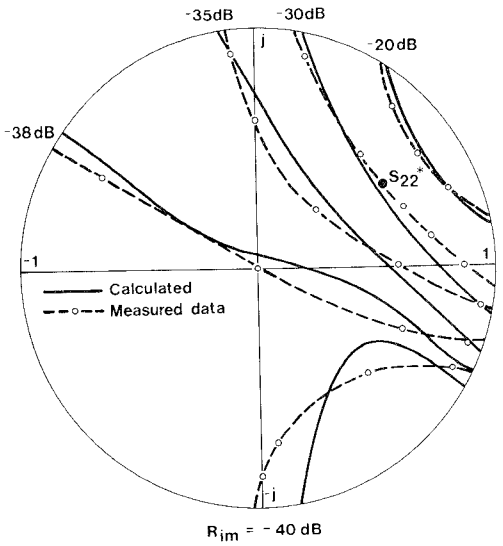

Fig. 5. Calculated and measured contours of constant small-signal third-order IMD ratio at 10 GHz on the load reflection coefficient plane.

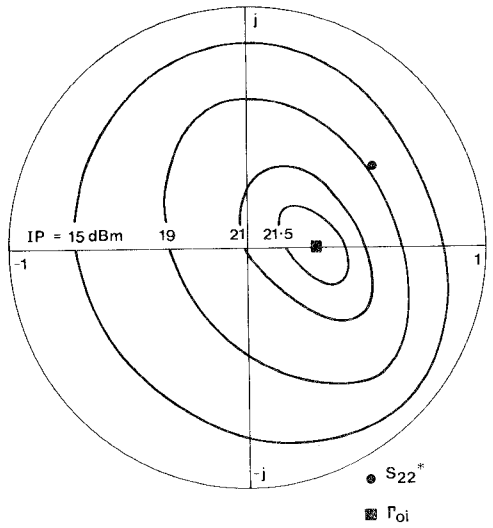

Fig. 6. Calculated contours of constant intercept point at 10 GHz on the load reflection coefficient plane.

Intermodulation Distortion

Fig. 5 shows calculated and experimental contours of constant small-signal IMD ratio R_{im} on the load reflection coefficient plane of the GaAs FET. These data have been presented previously [4] but are included here for completeness. The frequency is 10 GHz and the total two-tone input power is -4.83 dBm.[2] The three device-dependent parameters in (28) (magnitude and phase of E and magnitude of D) were obtained by least squares fitting the calculated R_{im} values to the measured data [4], [6]. Their values are $E=0.0754 \angle -99°$ and $|D|=0.0246$ for P_{in} expressed in milliwatts.

Comparing the relative magnitudes of the two terms within the modulus signs of (28) for various values of load admittance, it is possible to draw certain conclusions regarding the dominant source of distortion within the FET. For the particular transistor described here, the term involving $|D|$, which represents distortion at the drain, is largest in the region of conjugate match (S_{22}^*). The term involving E is dominant in the high-admittance region to the left of the output reflection coefficient plane. In a practical amplifier circuit, the output of the transistor is usually presented with a load which is close to S_{22}^*. Thus the nonlinear output (drain) admittance would be the dominant distortion-producing element.

Intercept Point

Using the device parameters given above, the intercept point of the GaAs FET was computed as a function of the load. Contours of constant intercept point were then plotted on the load reflection coefficient plane and are shown in Fig. 6. It is of interest to note that these are closed contours and that there is an optimum load reflection coefficient which gives the maximum intercept point. This optimum reflection coefficient Γ_{oi} was obtained by a simple numerical optimization of Y in (30) to maximize IP and is shown in Fig. 6. For the transistor considered here, Γ_{oi} happens to be real. In general, it will be complex. The maximum intercept point is 21.73 dBm, while the intercept point at the load for small-signal conjugate match (S_{22}^*) is 18.48 dBm. This indicates that an improvement of 3.25 dBm in the intercept point can be obtained by detuning the device from conjugate match to load for maximum intercept point. The corresponding reduction in small-signal gain is 2.11 dB.

Gain Compression

As shown in Section III, one requires four device parameters in order to calculate gain compression using (19). These four parameters (magnitude and phase of B and D) can be obtained from E and $|D|$ which were obtained from IMD measurements. The only additional information required is the phase angle of D. This angle was obtained from gain compression measurements with a 50-Ω load impedance connected to the device. A 50-Ω load was selected because it results in a relatively small amount of gain compression in the nonlinear output admittance. The input circuit thus had a strong influence on the overall gain compression, and the compression was sensitive to changes in the parameter B in (19). From (27) the magnitude of B is 0.0754. The phase was adjusted to give agreement between the calculated and measured gain compression. The resulting value of B is $0.0754 \angle -118°$ which in (27) gives $D=0.0246 \angle -19°$.

Fig. 7(a) shows the experimental and calculated output power versus input power characteristic of the FET at 10 GHz with a 50-Ω load and a single-tone input signal. A corresponding characteristic for a conjugate match at the output of the transistor is shown in Fig. 7(b). Agreement

[2]Equivalent to an available input power of -2 dBm from a 50-Ω input impedance.

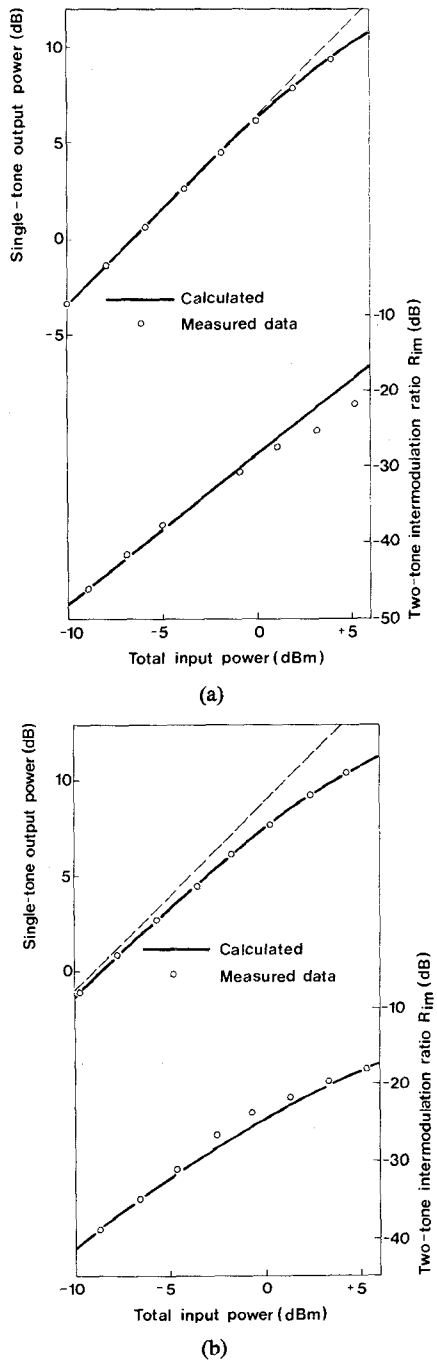

Fig. 7. Calculated and measured single-tone output power versus input power and two-tone IMD ratio versus total input power. The severity of gain compression can be gauged by the deviation of single-tone output power from the broken line, which is a linear extrapolation of the small-signal output power characteristic. (a) 50-Ω load impedance. (b) Conjugate match at the output.

between the calculated and measured data is good in both cases. Also shown in Fig. 7 is the measured third-order IMD ratio associated with a two-tone input signal of the same total power. This is compared with calculated values obtained from (26), again showing good agreement.

Calculated contours of constant gain compression $|k|^2$ on the load reflection coefficient plane of the transistor are shown in Fig. 8. These data were obtained directly from (19) but could equally well have been obtained from

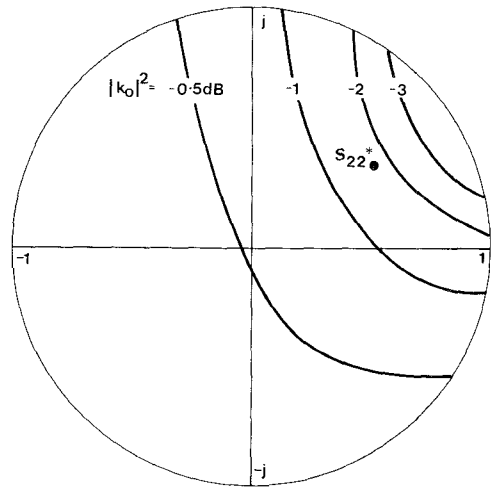

Fig. 8. Calculated contours of constant gain compression $|k|^2$ for an input power level of 4 dBm at 10 GHz.

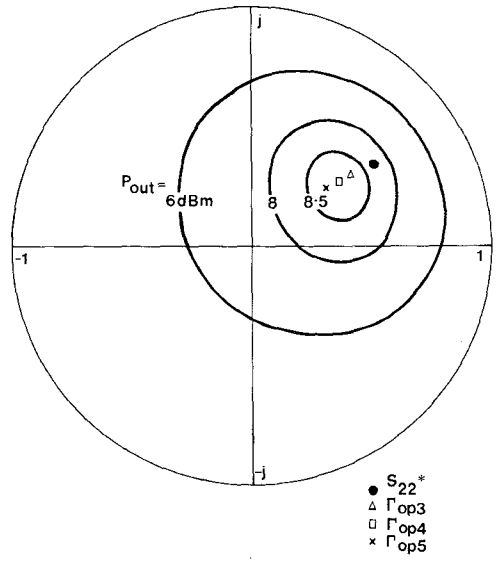

Fig. 9. Calculated contours of constant output power for an input power of 4 dBm at 10 GHz. Optimum load reflection coefficients for input powers of 3, 4, and 5 dBm are shown.

(20), (21), and the normalized curves of Fig. 2. The transistor is driven by a single-tone carrier with a constant available input power of 4 dBm at 10 GHz, and the source impedance is 50 Ω. Gain compression is considerable in the region of small-signal conjugate match (S_{22}^*), but approaches a value of −0.41 dB as the load tends towards a short circuit. This "short-circuit gain compression" is entirely due to the nonlinear input circuit of the FET since the output circuit gain compression $|k_o|^2$ approaches unity as the load admittance Y_L and the admittance $Y = Y_L + J_1$ becomes infinite.

Output Power Contours

Fig. 9 shows calculated contours of constant output power for the same constant available input power of 4 dBm at 10 GHz, computed from (16), (17), and (19). As with the contours of constant intercept point, they are

closed, and there is an optimum load reflection coefficient at which the output power is maximum. This maximum output power is 8.7 dBm, and the optimum reflection coefficient for the 4-dBm input power Γ_{op4} is shown. For a small-signal conjugate match at the output of the device, the output power for an input power of 4 dBm is 8.3 dBm, indicating that a 0.4-dB improvement in output power can be obtained by selecting a load reflection coefficient of Γ_{op4} rather than S_{22}^*.

In the design of high-efficiency amplifiers, an increase in the output power by as little as 0.4 dB represents a significant improvement. Knowledge of the optimum load reflection coefficient is thus of considerable importance. The reflection coefficients Γ_{op3} and Γ_{op5} in Fig. 9 are the loads for maximum output power at input power levels of 3 and 5 dBm, respectively. It can be seen that as the input power level is increased, the optimum load reflection coefficient moves away from S_{22}^*.

V. Conclusions

The analytical expressions for gain compression, AM-to-PM conversion, IMD ratio, and intercept point derived here are based on a simple unilateral nonlinear circuit model of the GaAs FET. It has been shown that by subdividing the circuit model into an input and an output circuit, the contribution of the nonlinearities at the gate and in the transconductance can be distinguished from the contribution of the nonlinearities at the drain. Normalized contours of constant gain compression and AM-to-PM conversion due to the drain nonlinearities in the output circuit have been presented. Examples of these distortion characteristics, together with third-order IMD ratio, intercept point and output power contours for constant input power have been given for a particular transistor. The theoretical IMD and gain compression characteristics both showed close agreement with experimental data. For the transistor considered, the theory predicts closed contours of constant intercept point and constant output power. Optimum loads for maximum intercept point and maximum output power have been given.

Values of the device parameters which characterize the nonlinearities in the transistor were obtained here from a series of IMD measurements as a function of the load and from a gain compression measurement. Alternatively, other measurement schemes can also be used. It is possible, for example, to obtain the device parameters from a series of gain compression measurements and a single IMD measurement.

The results presented here should find application in the analysis and design of low-distortion and high-efficiency amplifiers. Each of the distortion characteristics considered lends itself to presentation in graphical form and is thus compatible with conventional Smith chart techniques. In addition, since the analytical expressions for distortion characteristics are easily and quickly evaluated, they could readily be incorporated in a computer-aided optimization scheme.

VI. Appendix

The carrier-frequency component i_{xc} of the current i_x and the third-order IMD component i_{xd} of i_x are found by putting $N=3$ in (1) and substituting (2):

$$i_{xc} = Ag_{m1}\{\cos(\omega_1 t+\epsilon_1)+\cos(\omega_2 t+\epsilon_1)\} + \tfrac{3}{4}A^3 g_{m3}\{\cos(\omega_1 t+\epsilon_3)+\cos(\omega_2 t+\epsilon_3)\}$$

and

$$i_{xd} = \tfrac{3}{4}A^3 g_{m3}[\cos\{(2\omega_1-\omega_2)t+\epsilon_3\} + \cos\{(2\omega_2-\omega_1)t+\epsilon_3\}]$$

where

$$\epsilon_l = -\omega_1 \tau_l$$

and $\omega_1 \simeq \omega_2$. It follows directly that in phasor notation these currents are as given by (3) and (4).

For the *output circuit* the carrier and IMD components of I_g are found by substituting time-domain representations of V_{oc} and V_{od} into (7) and (8) with $N=3$, $g_2=c_2=0$, and using

$$i_y(t) = i_g(t)+i_c(t).$$

Thus for a two-tone input signal at the gate as given by (2)

$$I_{yc} = V_{oc}J_1\{1+\tfrac{9}{4}J_3J_1^{-1} \cdot(|V_{oc}|^2+\tfrac{1}{3}W_{od}+\text{term in } |V_{od}|^2)\} \quad \text{(A1)}$$

and

$$I_{yd} = V_{od}J_1+\tfrac{3}{4}V_{oc}J_3 \cdot(|V_{oc}|^2+2W_{od}+\text{term in } |V_{od}|^3|V_{oc}|^{-1}) \quad \text{(A2)}$$

where I_{yc} is the carrier-frequency component of I_y, I_{yd} is the third-order IMD component of I_y,

$$J_l = |J_l|\angle\sigma_l = g_l+j\omega_1 c_l$$

and

$$W_{od} = |V_{oc}|\{V_{od}+2\,\text{Re}\,(V_{od})\}.$$

For third-order IMD ratios less than about -20 dB (where $|V_{od}|/|V_{oc}|<10$), the terms in $|V_{od}|^2$ in (A1) and (A2) can be neglected and the term in W_{od} appearing in (A1) can be neglected. The expressions (A1) and (A2) thus simplify to (9) and (10).

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23-GHz Band GaAs MESFET Reflection-Type Amplifier

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***Abstract*—A new method is presented for applying a packaged GaAs MESFET to an amplifier in the frequency region above 20 GHz, using package resonance as a positive feedback element and operating GaAs MESFET as a negative resistance two-terminal device in a reflection-type amplifier. Experimentally, a 6-dB noise figure in the 23-GHz band and a 8-dB noise figure in the 27-GHz band have been achieved.**

I. Introduction

THE GaAs MESFET, as the only three-terminal device available in the frequency region above *X* band, is evolving into the higher frequency region. Several amplifiers using the GaAs MESFET in a 20-GHz band have been reported [1]–[3]. When developing a low-noise preamplifier in the higher frequency region, conventional MIC technology encounters difficulties because the loss in the input/interstage/output matching networks increases as the frequency goes higher than 20 GHz. In addition, the available gain per single stage in those high-frequency regions is not so high as to be insensitive to the noise and loss characteristics of the following stages. Because of these factors, the required number of cascaded stages for an amplifier increases, causing overall noise-figure degradation by interstage loss accumulation. The circuit loss problem can be overcome by using a waveguide circuit and directly coupling the waveguide and GaAs MESFET. The GaAs MESFET, a three-terminal device, can be operated as a negative resistance two-terminal device by properly terminating the gate–source port [2]. Thus the gain problem can be overcome by employing the resulting two-terminal device in a reflection-type amplifier. This paper describes the feasibility of a low-noise amplifier operating at frequencies higher than 20 GHz by employing a packaged GaAs MESFET in a waveguide as a reflection-type amplifier.

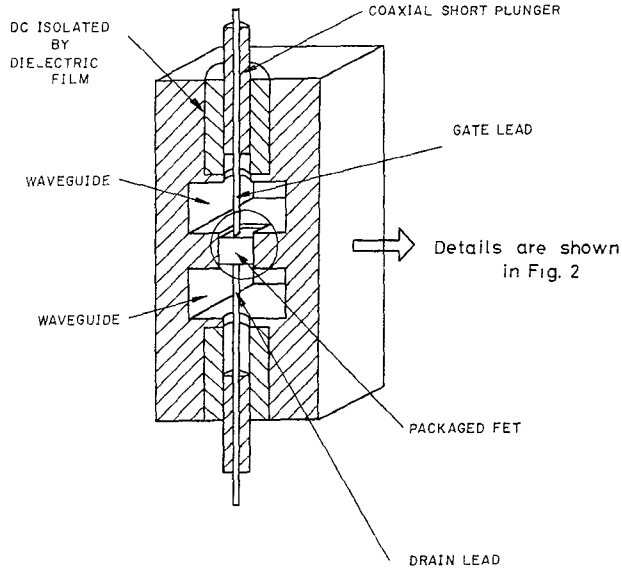

Fig. 1. Waveguide mount structure.

II. Experimental Work

A. GaAs MESFET Mounting

The waveguide mount shown in Fig. 1 was constructed to couple the GaAs MESFET and waveguides directly. The mount is composed of stacked waveguides, FET housing section (a form of through-hole between the stacked waveguides), and two transducers (gate/waveguide and drain/waveguide). Each transducer consists of a waveguide short plunger and a coaxial short plunger whose center conductor is soldered to gate/drain

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